## IN THE CLAIMS

Please delete claims 1-11 and add new claims 12-57 as follows:

12. A computer implemented device that simulates the electronic and optical characteristics of an integrated optical/electronic circuit, comprising:

an electronic design portion that simulates characteristics of at least certain electronic circuits of said integrated optical/electronic circuit, and generates topology information and free-carrier concentration information associated with the electronic circuits; and

an optical design portion that simulates characteristics of at least certain optical circuits of said integrated optical/electronic circuit in response to said topology information and said free-carrier concentration information generated by said electronic design portion.

13. The device of claim 12, wherein the electronic design portion includes a process simulation portion that generates said topology information.

14. The device of claim 12, wherein the electronic design portion includes a device simulation portion that generates said free-carrier concentration information.

15. The device of claim 12, wherein said electronic design portion includes at least one of the group consisting of a process simulation portion, a device simulation portion, a layout portion, a parasitic extraction portion, and a circuit simulation portion.

16. The device of claim 12, wherein said optical simulation portion further comprises at

least one of the group consisting of: a waveguide grating portion, a diffraction optical element portion, a finite difference time domain portion, a thin film portion, a beam propagation method portion, and a raytracing portion.

17. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a focusing mirror.

18. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a waveguide.

19. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a Fabry-Perot cavity.

20. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a wavelength division multiplexer modulator.

21. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as an evanescent coupler.

22. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a diode.

23. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a transistor.

24. The device of claim 12, wherein the integrated optical/electronic circuit is at least partially formed on a Silicon-On-Insulator (SOI) substrate.

25. The device of claim 24, wherein the topology information generated by the electronic design portion is generated from process limitations.

26. The device of claim 25, wherein said SOI substrate includes a substrate layer, and wherein said waveguide at least partially extends within said substrate layer.

27. The device of claim 12, wherein the optical design portion models one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

28. A computer-readable medium having stored therein a plurality of instructions, the plurality of instructions including instructions which, when executed by a computer processor, simulate the electrical characteristics and the optical characteristics of an integrated optical/electronic circuit, the computer software causing the computer processor to:

simulate, with an electronic design portion, operation of at least certain electronics

circuits of said integrated optical/electronic circuit, said electronic design portion generating topology information and free-carrier concentration information; and

simulate, with an optical simulation portion, operation of at least certain optical circuits of said integrated optical/electronic circuit in response to said topology information and said free-carrier concentration information generated by said electronic design portion.

29. The computer-readable medium of claim 28, wherein the electronic design portion includes a process simulation portion that generates said topology information.

30. The computer-readable medium of claim 28, wherein the electronic design portion includes a device simulation portion that generates said free-carrier concentration information.

31. The computer-readable medium of claim 28, wherein said electronic design portion includes at least one of the group consisting of a process simulation portion, a device simulation portion, a layout portion, a parasitic extraction portion, and a circuit simulation portion.

32. The computer-readable medium of claim 28, wherein said optical design portion further comprises at least one of the group consisting of: a waveguide grating portion, a diffraction optical element portion, a finite difference time domain portion, a thin film portion, a beam propagation method portion, and a raytracing portion.

33. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a focusing

mirror.

34. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a waveguide.

35. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a Fabry-Perot cavity.

36. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a wavelength division multiplexer modulator.

37. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including an evanescent coupler.

38. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a diode.

39. The computer-readable medium of claim 28, wherein the processor simulates the

operation of the optical characteristics of an integrated optical/electronic circuit as including a transistor.

40. The computer-readable medium of claim 28, wherein the integrated optical/electronic circuit is at least partially formed on a Silicon-On-Insulator (SOI) substrate.

41. The computer-readable medium of claim 40, wherein the optical design portion partially models a waveguide included in said at least certain optical circuits.

42. The computer-readable medium of claim 41, wherein said SOI substrate includes a substrate layer, and wherein said waveguide at least partially extends within said substrate layer.

43. The computer readable medium of claim 28, wherein the processor models the operation of one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

44. A method of operating a computer processor, the computer processor using computer software, the computer software is configured to simulate the electrical characteristics and the optical characteristics of an integrated optical/electronic circuit, the method comprising:

generating topology information and free-carrier concentration information by simulating operation of at least certain electronics circuits of said integrated optical/electronic circuit using an electronic design portion; and

simulating operation of at least certain optical circuits of said integrated optical/electronic

circuit in an optical design portion in response to said topology information and said free-carrier concentration information generated by said electronic design portion.

45. The method of claim 44, wherein the electronic design portion includes a process simulation portion that generates said topology information.

46. The method of claim 44, wherein the electronic design portion includes a device simulation portion that generates said free-carrier concentration information.

47. The method of claim 44, wherein said electronic design portion includes at least one of the group consisting of a process simulation portion, a device simulation portion, a layout portion, a parasitic extraction portion, and a circuit simulation portion.

48. The method of claim 44, wherein said optical design portion further comprises at least one of the group consisting of: a waveguide grating portion, a diffraction optical element portion, a finite difference time domain portion, a thin film portion, a beam propagation method portion, and a raytracing portion.

49. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including one from the group of a focusing mirror, a waveguide, and a Fabry-Perot cavity.

50. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a wavelength division multiplexer modulator.

51. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including an evanescent coupler.

52. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a diode.

53. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a transistor.

54. The method of claim 44, wherein the integrated optical/electronic circuit is at least partially formed on a Silicon-On-Insulator (SOI) substrate.

55. The method of claim 54, wherein the optical simulation design tools portion partially models a waveguide included in said at least certain optical circuits.

56. The method of claim 55, wherein said SOI substrate includes a substrate layer, and

wherein said waveguide at least partially extends within said substrate layer.

57. The method of claim 44, wherein the computer processor modeling computer software simulates one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

## IN THE DRAWINGS

Applicant respectfully requests the Examiner's approval of the proposed changes to the drawing figures 5, 13, 20, 21, 22, 30, 47, 51, 52, 59, 60, 68A, 68B, 68C, 68D, 73, 74, 75, 76, 77, 78, 82, 83 and 88 in the request for Approval of Drawing Changes filed concurrently herewith.